16-Channel, 12-Bit Voltage-Output DAC with 14-Bit Increment Mode

AD5516*

FEATURES

High Integration:
16-Channel DAC in 12 mm × 12 mm CSPBGA
14-Bit Resolution via Increment/Decrement Mode
Guaranteed Monotonic
Low Power, SPI®, QSPI™, MICROWIRE™, and DSP Compatible
3-Wire Serial Interface
Output Impedance 0.5 Ω
Output Voltage Range
±2.5 V (AD5516-1)
±5 V (AD5516-2)
±10 V (AD5516-3)
Asynchronous Reset Facility (via $\overline{\text{RESET}}$ Pin)
Asynchronous Power-Down Facility (via PD Pin)
Daisy-Chain Mode
Temperature Range: –40°C to +85°C

APPLICATIONS

Level Setting
Instrumentation
Automatic Test Equipment
Optical Networks
Industrial Control Systems
Data Acquisition
Low Cost I/O

GENERAL DESCRIPTION

The AD5516 is a 16-channel, 12-bit voltage-output DAC. The selected DAC register is written to via the 3-wire serial interface. DAC selection is accomplished via address bits A3–A0. 14-bit resolution can be achieved by fine adjustment in Increment/Decrement Mode (Mode 2). The serial interface operates at clock rates up to 20 MHz and is compatible with standard SPI, MICROWIRE, and DSP interface standards. The output voltage range is fixed at ±2.5 V (AD5516-1), ±5 V (AD5516-2), and ±10 V (AD5516-3). Access to the feedback resistor in each channel is provided via the $R_{FB}0$ to $R_{FB}15$ pins.

The device is operated with AV_{CC} = 5 V ± 5%, DV_{CC} = 2.7 V to 5.25 V, V_{SS} = –4.75 V to –12 V, and V_{DD} = +4.75 V to +12 V, and requires a stable 3 V reference on REF_IN.

PRODUCT HIGHLIGHTS

1. Sixteen 12-bit DACs in one package, guaranteed monotonic.
2. Available in a 74-lead CSPBGA package with a body size of 12 mm × 12 mm.

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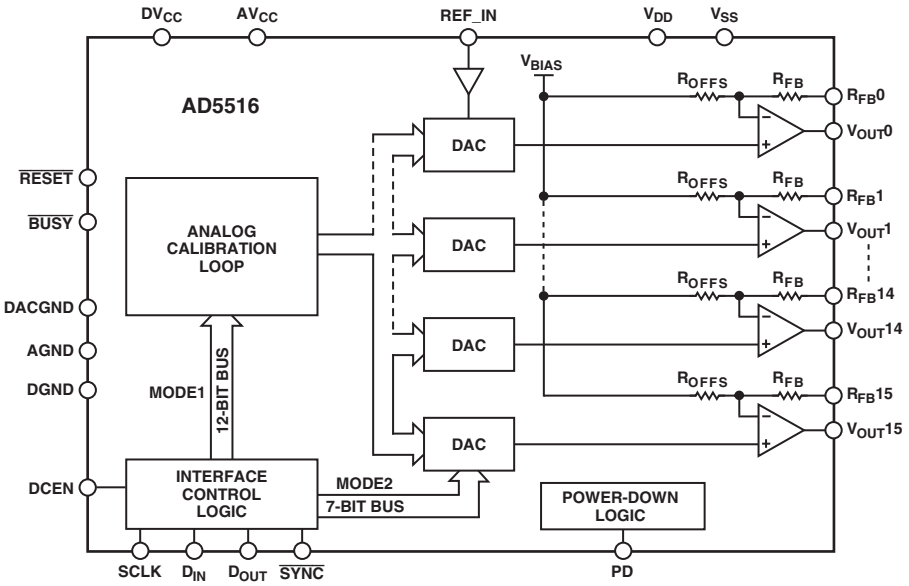
FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No. 5,969,657; other patents pending.

REV. B

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AD5516–SPECIFICATIONS

(V_{DD} = +4.75 V to +13.2 V, V_{SS} = –4.75 V to –13.2 V; AV_{CC} = 4.75 V to 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DACGND = 0 V; REF_IN = 3 V; All outputs unloaded. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter[1]	A Version[2]	Unit	Conditions/Comments
DAC DC PERFORMANCE			
Resolution	12	Bits	
Integral Nonlinearity (INL)	±2	LSB max	Mode 1
Differential Nonlinearity (DNL)	–1/+1.3	LSB max	±0.5 LSB typ, Monotonic; Mode 1
Increment/Decrement Step-Size	±0.25	LSB typ	Monotonic; Mode 2 Only
Bipolar Zero Error	±7	LSB max	
Positive Full-Scale Error	±10	LSB max	
Negative Full-Scale Error	±10	LSB max	
VOLTAGE REFERENCE			
REF_IN			
Nominal Input Voltage	3	V	
Input Voltage Range[3]	2.875/3.125	V min/max	
Input Current	±1	µA max	< 1 nA typ
ANALOG OUTPUTS (V_{OUT}0–15)			
Output Temperature Coefficient[3, 4]	10	ppm/°C typ	of FSR
DC Output Impedance[3]	0.5	Ω typ	
Output Range[5]			
AD5516-1	±2.5	V typ	100 µA Output Load
AD5516-2	±5	V typ	100 µA Output Load
AD5516-3	±10	V typ	100 µA Output Load
Resistive Load[3, 6, 7]	5	kΩ min	
Capacitive Load[3, 6]	200	pF	
Short Circuit Current[3]	7	mA typ	
DC Power Supply Rejection Ratio[3]	–85	dB typ	V_{DD} = +12 V ± 5%, V_{SS} = –12 V ± 5%
DC Crosstalk[3]	0.1	LSB max	
DIGITAL INPUTS[3]			
Input Current	±10	µA max	±5 µA typ
Input Low Voltage	0.8	V max	DV_{CC} = 5 V ± 5%
	0.4	V max	DV_{CC} = 3 V ± 10%
Input High Voltage	2.4	V min	DV_{CC} = 5 V ± 5%
	2	V min	DV_{CC} = 3 V ± 10%
Input Hysteresis (SCLK and $\overline{SYNC}$)	150	mV typ	
Input Capacitance	10	pF max	5 pF typ
DIGITAL OUTPUTS ($\overline{BUSY}$, D_{OUT})[3]			
Output Low Voltage, DV_{CC} = 5 V	0.4	V max	Sinking 200 µA
Output High Voltage, DV_{CC} = 5 V	4	V min	Sourcing 200 µA
Output Low Voltage, DV_{CC} = 3 V	0.4	V max	Sinking 200 µA
Output High Voltage, DV_{CC} = 3 V	2.4	V min	Sourcing 200 µA
High Impedance Leakage Current (D_{OUT} only)	±1	µA max	DCEN = 0
High Impedance Output Capacitance (D_{OUT} only)	5	pF typ	DCEN = 0
POWER REQUIREMENTS			
Power Supply Voltages			
V_{DD}	4.75/15.75	V min/max	
V_{SS}	–4.75/–15.75	V min/max	
AV_{CC}	4.75/5.25	V min/max	
DV_{CC}	2.7/5.25	V min/max	
Power Supply Currents[8]			
I_{DD}	5	mA max	3.5 mA typ. All Channels Full-Scale.
I_{SS}	5	mA max	3.5 mA typ. All Channels Full-Scale.
AI_{CC}	17	mA max	13 mA typ
DI_{CC}	1.5	mA max	1 mA typ
Power-Down Currents[8]			
I_{DD}	1	µA typ	
I_{SS}	1	µA typ	
AI_{CC}	2	µA max	200 nA typ
DI_{CC}	2	µA max	200 nA typ
Power Dissipation[8]	105	mW typ	V_{DD} = +5 V, V_{SS} = –5 V

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NOTES

[1] See Terminology section.

[2] A Version: Industrial temperature range –40°C to +85°C; typical at +25°C.

[3] Guaranteed by design and characterization; not production tested.

[4] AD780 as reference for the AD5516.

[5] Output range is restricted from V_{SS} + 2 V to V_{DD} – 2 V. Output span varies with reference voltage and is functional down to 2 V.

[6] Ensure that you do not exceed $T_{J\,(MAX)}$. See Absolute Maximum Ratings section.

[7] With 5 kΩ resistive load, footroom required is as follows: AD5516–1, 2 V; AD5516–2, 2.5 V; AD5516–3, 3 V.

[8] Outputs unloaded.

Specifications subject to change without notice.

AC CHARACTERISTICS

(V_{DD} = +4.75 V to +13.2 V, V_{SS} = –4.75 V to –13.2 V; AV_{CC} = 4.75 V to 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DACGND = 0 V; REF IN = 3 V. All outputs unloaded. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter[1, 2]	A Version[3]	Unit	Conditions/Comments
Output Voltage Settling Time (Mode 1)[4]			100 pF, 5 kΩ Load Full-Scale Change
AD5516–1	32	μs max	
AD5516–2	32	μs max	
AD5516–3	36	μs max	
Output Voltage Settling Time (Mode 2)[4]			100 pF, 5 kΩ Load, 127 Code Increment
AD5516–1	2.5	μs max	
AD5516–2	3.35	μs max	
AD5516–3	7	μs max	
Slew Rate	0.85	V/μs typ	
Digital-to-Analog Glitch Impulse	1	nV-s typ	1 LSB Change around Major Carry
Digital Crosstalk	5	nV-s typ	
Analog Crosstalk			
AD5516–1	1	nV-s typ	
AD5516–2	5	nV-s typ	
AD5516–3	20	nV-s typ	
Digital Feedthrough	1	nV-s typ	
Output Noise Spectral Density @ 10 kHz			
AD5516–1	150	nV/(Hz)$^{1/2}$ typ	
AD5516–2	350	nV/(Hz)$^{1/2}$ typ	
AD5516–3	700	nV/(Hz)$^{1/2}$ typ	

NOTES
[1]See Terminology section.
[2]Guaranteed by design and characterization; not production tested.
[3]A version: Industrial temperature range –40°C to +85°C.
[4]Timed from the end of a write sequence and includes $\overline{BUSY}$ low time.

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TIMING CHARACTERISTICS

(V_{DD} = +4.75 V to +13.2 V, V_{SS} = – 4.75 V to –13.2 V; AV_{CC} = 4.75 V to 5.25 V; DV_{CC} = 2.7 V to 5.25 V; AGND = DGND = DACGND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX} (A Version)	Unit	Conditions/Comments
$f_{UPDATE1}$	32	kHz max	DAC Update Rate (Mode 1)
$f_{UPDATE2}$	750	kHz max	DAC Update Rate (Mode 2)
f_{CLKIN}	20	MHz max	SCLK Frequency
t_1	20	ns min	SCLK High Pulsewidth
t_2	20	ns min	SCLK Low Pulsewidth
t_3	15	ns min	$\overline{SYNC}$ Falling Edge to SCLK Falling Edge Setup Time
t_4	5	ns min	D_{IN} Setup Time
t_5	5	ns min	D_{IN} Hold Time
t_6	0	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge
t_7	10	ns min	Minimum $\overline{SYNC}$ High Time (Standalone Mode)
t_{7MODE2}	400	ns min	Minimum $\overline{SYNC}$ High Time (Daisy-Chain Mode)
t_{8MODE1}	10	ns min	$\overline{BUSY}$ Rising Edge to $\overline{SYNC}$ Falling Edge
t_{9MODE2}	200	ns min	18th SCLK Falling Edge to $\overline{SYNC}$ Falling Edge (Standalone Mode)
t_{10}	10	ns min	$\overline{SYNC}$ Rising Edge to SCLK Rising Edge (Daisy-Chain Mode)
t_{11}[4]	20	ns max	SCLK Rising Edge to D_{OUT} Valid (Daisy-Chain Mode)
t_{12}	20	ns min	$\overline{RESET}$ Pulsewidth

NOTES
[1]See Timing Diagrams in Figures 1 and 2.
[2]Guaranteed by design and characterization; not production tested.
[3]All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[4]This is measured with the load circuit of Figure 3.

Specifications subject to change without notice.

TIMING DIAGRAMS

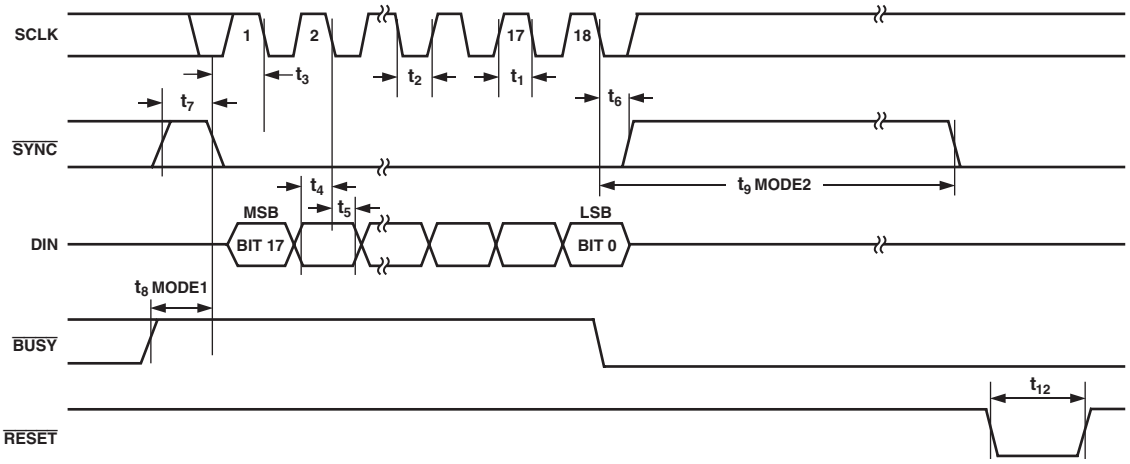

Figure 1. Serial Interface Timing Diagram

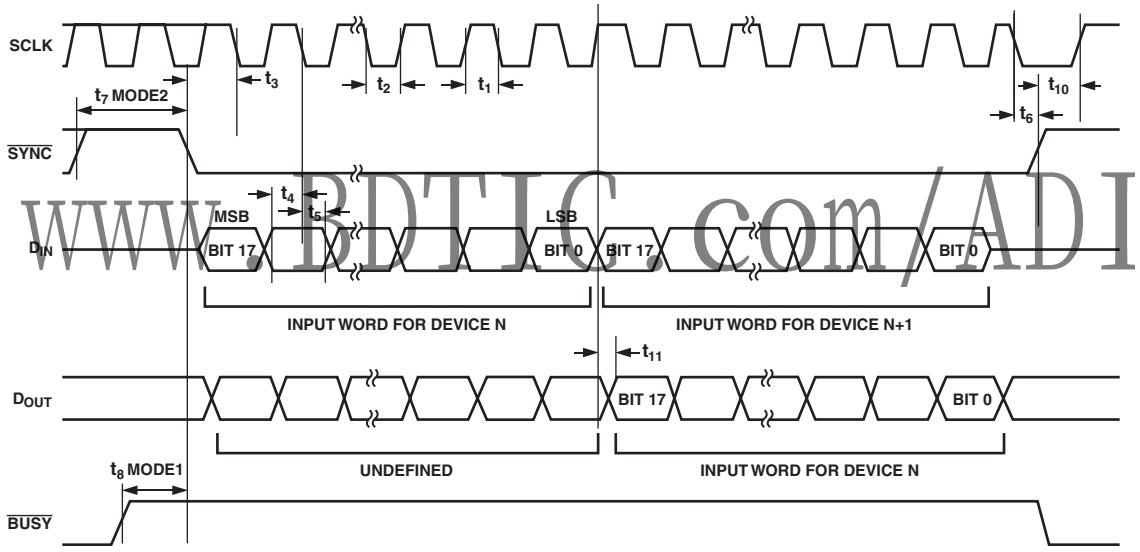

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Figure 2. Daisy-Chaining Timing Diagram

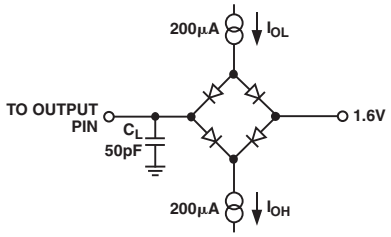

Figure 3. Load Circuit for D_{OUT} Timing Specifications

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to AGND . . . . . –0.3 V to +17 V
V_{SS} to AGND . . . . . +0.3 V to –17 V
AV_{CC} to AGND, DACGND . . . . . –0.3 V to +7 V
DV_{CC} to DGND . . . . . –0.3 V to +7 V
Digital Inputs to DGND . . . . . –0.3 V to DV_{CC} + 0.3 V
Digital Outputs to DGND . . . . . –0.3 V to DV_{CC} + 0.3 V
REF_IN to AGND, DACGND . . . . . –0.3 V to AV_{CC} + 0.3 V
V_{OUT}0–15 to AGND . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
AGND to DGND . . . . . –0.3 V to +0.3 V
R_{FB}0–15 to AGND . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
Operating Temperature Range, Industrial . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature ($T_{J\ MAX}$) . . . . . 150°C
74-Lead CSPBGA Package, θ_{JA} Thermal Impedance . . . 41°C/W
Reflow Soldering
Peak Temperature . . . . . 220°C
Time at Peak Temperature . . . . . 10 sec to 40 sec

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Function	Output Voltage Span	Package Option
AD5516ABC-1	16 DACs	±2.5 V	74-Lead CSPBGA
AD5516ABC-2	16 DACs	±5 V	74-Lead CSPBGA
AD5516ABC-3	16 DACs	±10 V	74-Lead CSPBGA
EVAL-AD5516-1EB			Evaluation Board
EVAL-AD5516-2EB			Evaluation Board
EVAL-AD5516-3EB			Evaluation Board

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5516 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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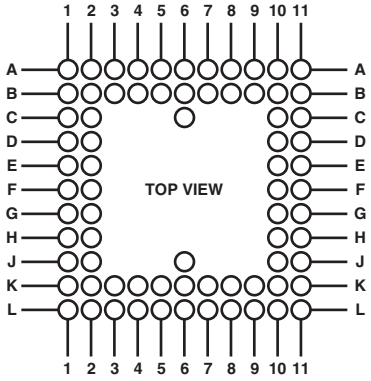
PIN CONFIGURATION



74-LEAD CSPBGA BALL CONFIGURATION

CSPBGA Number	Ball Name	CSPBGA Number	Ball Name	CSPBGA Number	Ball Name	CSPBGA Number	Ball Name	CSPBGA Number	Ball Name
A1	NC	B5	DGND	D11	NC	H10	$V_{OUT}13$	K9	$R_{FB}10$
A2	NC	B6	DGND	E1	$V_{OUT}1$	H11	$V_{OUT}12$	K10	$R_{FB}9$
A3	$\overline{RESET}$	B7	NC	E2	NC	J1	$R_{FB}3$	K11	$V_{OUT}11$
A4	$\overline{BUSY}$	B8	NC	E10	AGND1	J2	$V_{OUT}4$	L1	NC
A5	DGND	B9	SCLK	E11	PD	J6	NC	L2	$V_{OUT}6$
A6	DV_{CC}	B10	NC	F1	$V_{OUT}2$	J10	$R_{FB}12$	L3	$R_{FB}6$
A7	D_{OUT}	B11	REF_IN	F2	$R_{FB}1$	J11	$R_{FB}11$	L4	$V_{OUT}7$
A8	D_{IN}	C1	$V_{OUT}0$	F10	AGND2	K1	$R_{FB}4$	L5	NC
A9	$\overline{SYNC}$	C2	DACGND	F11	$R_{FB}14$	K2	$V_{OUT}5$	L6	$V_{DD}2$
A10	NC	C6	NC	G1	$R_{FB}2$	K3	$R_{FB}5$	L7	$V_{DD}1$
A11	NC	C10	$AV_{CC}1$	G2	$R_{FB}15$	K4	NC	L8	$R_{FB}7$
B1	NC	C11	NC	G10	$V_{OUT}14$	K5	$V_{SS}2$	L9	$V_{OUT}8$
B2	NC	D1	$R_{FB}0$	G11	$R_{FB}13$	K6	$V_{SS}1$	L10	$R_{FB}8$
B3	NC	D2	DACGND	H1	$V_{OUT}3$	K7	$V_{OUT}10$	L11	NC
B4	DCEN	D10	$AV_{CC}2$	H2	$V_{OUT}15$	K8	$V_{OUT}9$		

NC = Not Internally Connected

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PIN FUNCTION DESCRIPTIONS

Mnemonic	Function
AGND (1–2)	Analog GND Pins
AV_{CC} (1–2)	Analog Supply Pins. Voltage range from 4.75 V to 5.25 V.
V_{DD} (1–2)	V_{DD} Supply Pins. Voltage range from 4.75 V to 15.75 V.
V_{SS} (1–2)	V_{SS} Supply Pins. Voltage range from –4.75 V to –15.75 V.
DGND	Digital GND Pins
DV_{CC}	Digital Supply Pin. Voltage range from 2.7 V to 5.25 V.
DACGND	Reference GND Supply for All 16 DACs
REF_IN	Reference Input Voltage for All 16 DACs. The recommended value of REF_IN is 3 V.
V_{OUT} (0–15)	Analog Output Voltages from the 16 DAC Channels
R_{FB} (0–15)	Feedback Resistors. For nominal output voltage range, connect each R_{FB} to its corresponding V_{OUT}. Access to the feedback resistors enables the user to increase the DAC current drive or generate programmable current sources. They should not be used for gain adjustment.
$\overline{SYNC}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred in on the falling edge of SCLK.

PIN FUNCTION DESCRIPTIONS (continued)

Mnemonic	Function
SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 20 MHz.
D_{IN}	Serial Data Input. Data must be valid on the falling edge of SCLK.
D_{OUT}	Serial Data Output. D_{OUT} can be used for daisy-chaining a number of devices together or for reading back the data in the shift register for diagnostic purposes. Data is clocked out on D_{OUT} on the rising edge of SCLK and is valid on the falling edge of SCLK.
DCEN[1]	Active High Control Input. This pin is tied high to enable Daisy-Chain Mode.
$\overline{RESET}$[2]	Active Low Control Input. This resets all DAC registers to power-on value.
PD[1]	Active High Control Input. All DACs go into power-down mode when this pin is high. The DAC outputs go into a high impedance state.
$\overline{BUSY}$	Active Low Output. This signal tells the user that the analog calibration loop is active. It goes low during conversion. The duration of the pulse on $\overline{BUSY}$ determines the maximum DAC update rate, f_{UPDATE}. Further writes to the AD5516 are ignored while $\overline{BUSY}$ is active.

NOTES
[1]Internal pull-down device on this logic input. Therefore it can be left floating and will default to a logic low condition.
[2]Internal pull-up device on this logic input. Therefore it can be left floating and will default to a logic high condition.

TERMINOLOGY

Integral Nonlinearity (INL)
This is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is expressed in LSBs.

Differential Nonlinearity (DNL)
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of –1 LSB maximum ensures monotonicity.

Bipolar Zero Error
Bipolar zero error is the deviation of the DAC output from the ideal midscale of 0 V. It is measured with 10...00 loaded to the DAC. It is expressed in LSBs.

Positive Full-Scale Error
This is the error in the DAC output voltage with all 1s loaded to the DAC. Ideally the DAC output voltage, with all 1s loaded to the DAC registers, should be 2.5 V – 1 LSB (AD5516-1), 5 V – 1 LSB (AD5516-2), and 10 V – 1 LSB (AD5516-3). It is expressed in LSBs.

Negative Full-Scale Error
This is the error in the DAC output voltage with all 0s loaded to the DAC. Ideally the DAC output voltage, with all 0s loaded to the DAC registers, should be –2.5 V (AD5516-1), –5 V (AD5516-2), and –10 V (AD5516-3). It is expressed in LSBs.

Output Temperature Coefficient
This is a measure of the change in analog output with changes in temperature. It is expressed in ppm/°C of FSR.

DC Power Supply Rejection Ratio
DC power supply rejection ratio (PSRR) is a measure of the change in analog output for a change in supply voltage (V_{DD} and V_{SS}). It is expressed in dB. V_{DD} and V_{SS} are varied ±5%.

DC Crosstalk
This is the dc change in the output level of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) and output change of another DAC. It is expressed in LSB.

Output Settling Time
This is the time taken from when the last data bit is clocked into the DAC until the output has settled to within ±0.5 LSB of its final value (see TPC 7).

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Digital-to-Analog Glitch Impulse
This is the area of the glitch injected into the analog output when the code in the DAC register changes state. It is specified as the area of the glitch in nV-s when the digital code is changed by 1 LSB at the major carry transition (011...11 to 100...00 or 100...00 to 011...11).

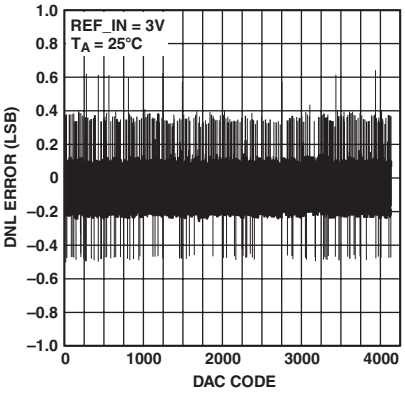
Digital Crosstalk
This is the glitch impulse transferred to the output of one DAC at midscale while a full-scale code change (all 1s to all 0s and vice versa) is being written to another DAC. It is expressed in nV-s.

Analog Crosstalk
This is the area of the glitch transferred to the output (V_{OUT}) of one DAC due to a full-scale change in the output (V_{OUT}) of another DAC. The area of the glitch is expressed in nV-s.

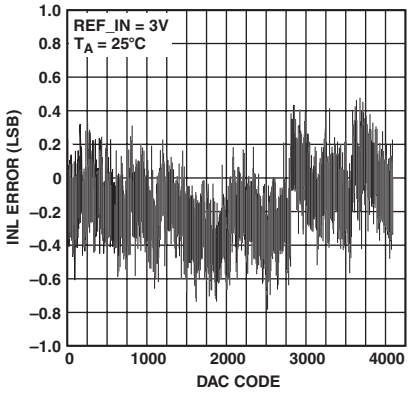
Digital Feedthrough
This is a measure of the impulse injected into the analog outputs from the digital control inputs when the part is not being written to, i.e., SYNC is high. It is specified in nV-s and measured with a worst-case change on the digital input pins, e.g., from all 0s to all 1s and vice versa.

Output Noise Spectral Density
This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per root hertz). It is measured in nV/(Hz)$^{1/2}$.

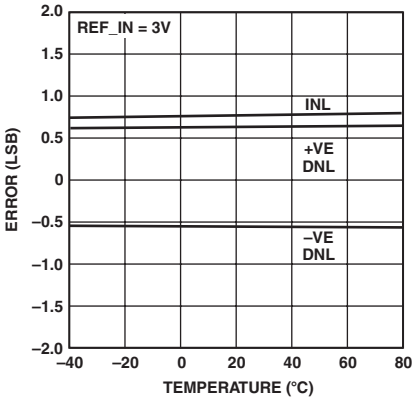
AD5516–Typical Performance Characteristics



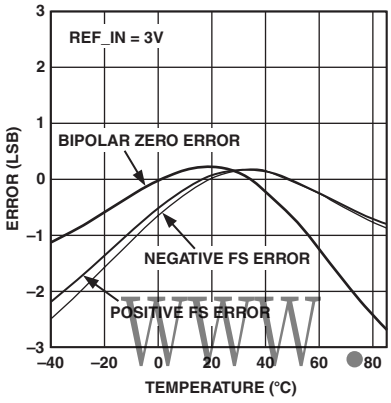
TPC 1. Typical DNL Plot



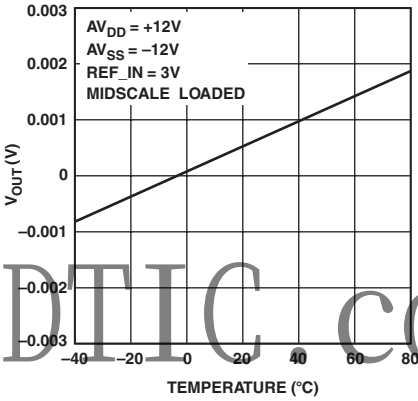
TPC 2. Typical INL Plot



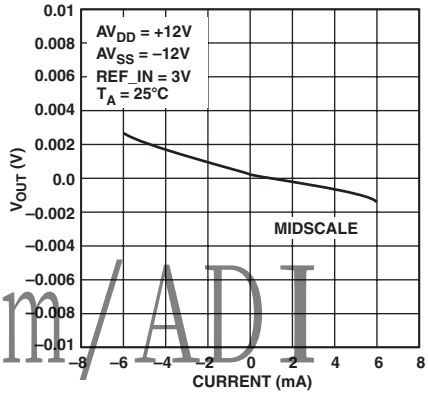
TPC 3. Typical INL Error and DNL Error vs. Temperature



TPC 4. Bipolar Zero Error and Full-Scale Error vs. Temperature



TPC 5. V_{OUT} vs. Temperature



TPC 6. V_{OUT} Source and Sink Capability

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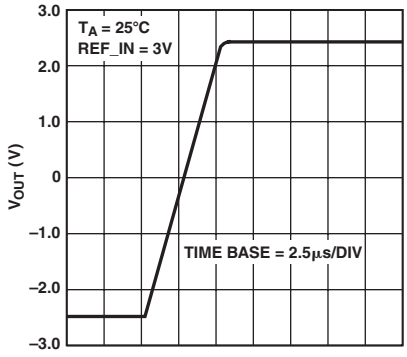
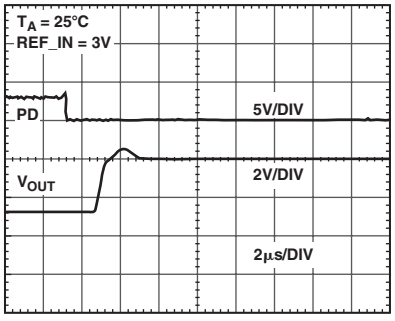
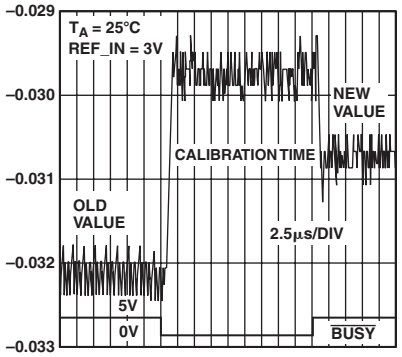


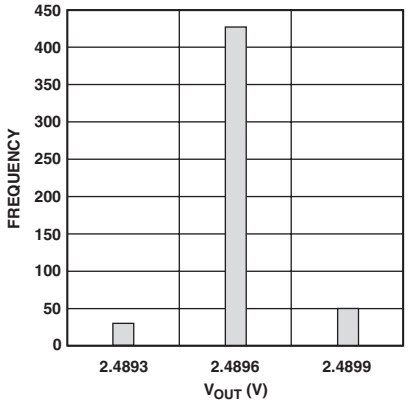
TPC 7. AD5516–1 Full-Scale Settling Time



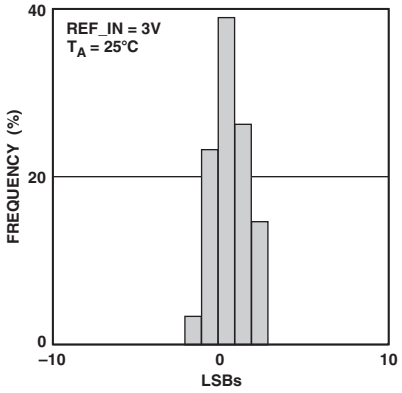
TPC 8. Exiting Power-Down to Full Scale



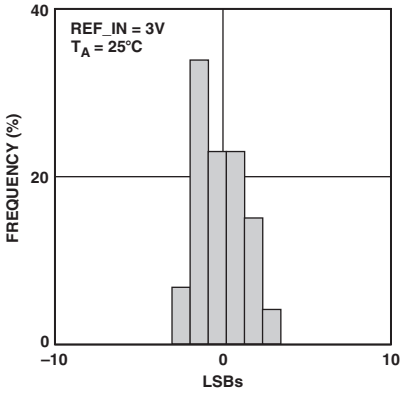
TPC 9. AD5516–1 Major Code Transition Glitch Impulse



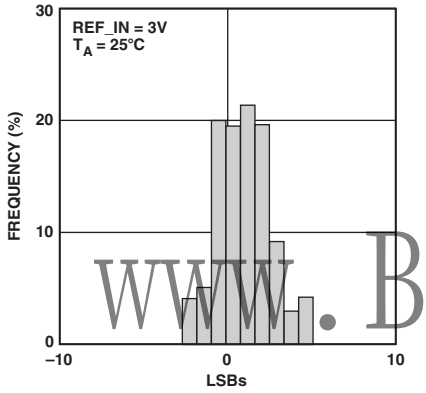
TPC 10. AD5516–1 V_{OUT} Repeatability; Programming the Same Code Multiple Times



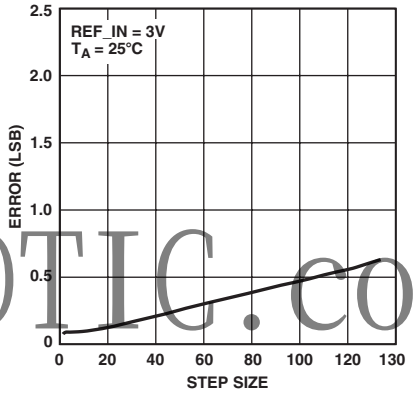
TPC 11. Bipolar Error Distribution



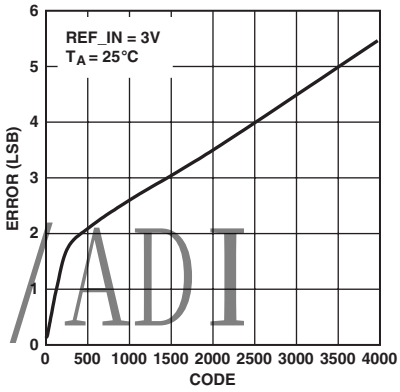
TPC 12. Positive Full-Scale Error Distribution



TPC 13. Negative Full-Scale Error Distribution



TPC 14. Accuracy vs. Increment Step



TPC 15. Accuracy vs. Increment Step, Using All 12 Mode 2 Bits

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FUNCTIONAL DESCRIPTION

The AD5516 consists of sixteen 12-bit DACs in a single package. A single reference input pin (REF_IN) is used to provide a 3 V reference for all 16 DACs. To update a DAC's output voltage, the required DAC is addressed via the 3-wire serial interface. Once the serial write is complete, the selected DAC converts the code into an output voltage. The output amplifiers translate the DAC output range to give the appropriate voltage range (±2.5 V, ±5 V, or ±10 V) at output pins $V_{OUT}0$ to $V_{OUT}15$.

The AD5516 uses a self-calibrating architecture to achieve 12-bit performance. The calibration routine servos to select the appropriate voltage level on an internal 14-bit resolution DAC. $\overline{BUSY}$ output goes low for the duration of the calibration and further writes to the AD5516 are ignored while $\overline{BUSY}$ is low. $\overline{BUSY}$ low time is typically 25 µs. Noise during the calibration ($\overline{BUSY}$ low period) can result in the selection of a voltage within a ±0.25 LSB band around the normal selected voltage. See TPC 10.

It is essential to minimize noise on REFIN for optimal performance. The AD780's specified decoupling makes it the ideal reference to drive the AD5516.

Upon power-on, all DACs power up to a reset value (see the RESET section).

DIGITAL-TO-ANALOG SECTION

The architecture of each DAC channel consists of a resistor string DAC followed by an output buffer amplifier with offset and gain. The voltage at the REF_IN pin provides the reference voltage for all 16 DACs. The input coding to the DACs is offset binary; this results in ideal output voltages as follows:

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AD5516-1: $$V_{OUT} = \frac{2 \times V_{REF\_IN} \times 2.5 \times D}{3 \times 2^N} - \frac{V_{REF\_IN} \times 2.5}{3}$$

AD5516-2: $$V_{OUT} = \frac{4 \times V_{REF\_IN} \times 2.5 \times D}{3 \times 2^N} - \frac{2 V_{REF\_IN} \times 2.5}{3}$$

AD5516-3: $$V_{OUT} = \frac{8 \times V_{REF\_IN} \times 2.5 \times D}{3 \times 2^N} - \frac{4 V_{REF\_IN} \times 2.5}{3}$$

Where:

D = decimal equivalent of the binary code that is loaded to the DAC register, i.e., 0–4095

N = DAC resolution = 12

Table I illustrates ideal analog output versus DAC code.

Table I. DAC Register Contents AD5516-1

MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$V_{REF\_IN} \times 2.5/3 - 1$ LSB
1000 0000 0000	0 V
0000 0000 0000	$-V_{REF\_IN} \times 2.5/3$

MODES OF OPERATION

The AD5516 has two modes of operation.

Mode 1 (MODE bits = 00): The user programs a 12-bit dataword to one of 16 channels via the serial interface. This word is loaded into the addressed DAC register and is then converted into an analog output voltage. During conversion, the $\overline{BUSY}$ output is low and all SCLK pulses are ignored. At the end of a conversion $\overline{BUSY}$ goes high, indicating that the update of the addressed DAC is complete. It is recommended that SCLK is not pulsed while $\overline{BUSY}$ is low. Mode 1 conversion takes 25 µs typ.

Mode 2 (MODE bits = 01 or 10): Mode 2 operation allows the user to increment or decrement the DAC output in 0.25 LSB steps, resulting in a 14-bit monotonic DAC. The amount by which the DAC output is incremented or decremented is determined by Mode 2 bits DB11–DB0, e.g., for a 0.25 LSB increment/decrement DB11...DB0 = 0000 0000 0001, while for a 2.5 LSB increment/decrement, DB11...DB0 = 0000 0000 1010. The MODE bits determine whether the DAC data is incremented (01) or decremented (10). The maximum amount that the user is allowed to increment or decrement the DAC output is 4095 steps of 0.25 LSB, i.e., DB11...DB0 = 1111 1111 1111. Mode 2 update takes approximately 1 µs. The Mode 2 feature allows increased resolution, but overall increment/decrement accuracy varies with increment/decrement step as shown in TPC 14 and TPC 15.

Mode 2 is useful in applications where greater resolution is required, for example, in servo applications requiring fine-tune to 14-bit resolution.

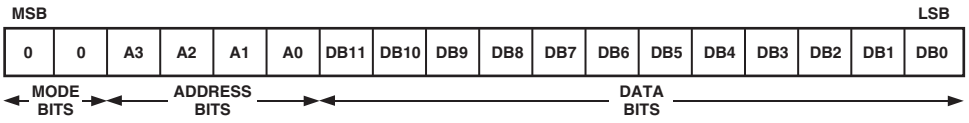

Figure 4. Mode 1 Data Format

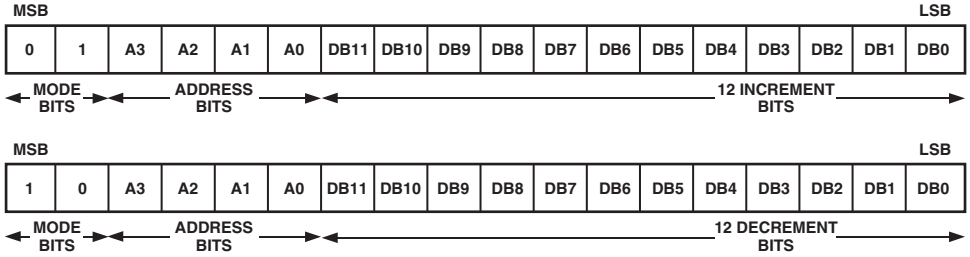
MSB
LSB
0 1 A3 A2 A1 A0 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
MODE BITS
ADDRESS BITS
12 INCREMENT BITS
MSB
LSB
1 0 A3 A2 A1 A0 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
MODE BITS
ADDRESS BITS
12 DECREMENT BITS

Figure 5. Mode 2 Data Format

The user must allow 200 ns (min) between two consecutive Mode 2 writes in Standalone Mode and 400 ns (min) between two consecutive Mode 2 writes in Daisy-Chain Mode. During a Mode 2 operation the $\overline{BUSY}$ signal remains high.

See Figures 4 and 5 for Mode 1 and Mode 2 data formats.

When MODE bits = 11, the device is in No Operation mode. This may be useful in daisy-chain applications where the user does not wish to change the settings of the DACs. Simply write 11 to the MODE bits and the following address and data bits will be ignored.

SERIAL INTERFACE

The AD5516 has a 3-wire interface that is compatible with SPI/QSPI/MICROWIRE, and DSP interface standards. Data is written to the device in 18-bit words. This 18-bit word consists of two mode bits, four address bits, and 12 data bits as shown in Figure 4.

The serial interface works with both a continuous and burst clock. The first falling edge of $\overline{SYNC}$ resets a counter that counts the number of serial clocks to ensure the correct number of bits is shifted in and out of the serial shift registers. In order for another serial transfer to take place, the counter must be reset by the falling edge of $\overline{SYNC}$.

A3–A0

Four address bits (A3 = MSB Address, A0 = LSB). These are used to address one of 16 DACs.

Table II. Selected DAC

A3	A2	A1	A0	Selected DAC
0	0	0	0	DAC 0
0	0	0	1	DAC 1
:	:	:	:	
1	1	1	1	DAC 15

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DB11–DB0

These are used to write a 12-bit word into the addressed DAC register. Figures 1 and 2 show the timing diagram for a write cycle to the AD5516.

$\overline{SYNC}$ FUNCTION

In both Standalone and Daisy-Chain Modes, $\overline{SYNC}$ is an edge-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low observing the minimum $\overline{SYNC}$ falling to SCLK falling edge setup time, t_3.

Standalone Mode (DCEN = 0)

After $\overline{SYNC}$ goes low, serial data will be shifted into the device's input shift register on the falling edges of SCLK for 18 clock pulses. After the falling edge of the 18th SCLK pulse, data will automatically be transferred from the input shift register to the addressed DAC.

$\overline{SYNC}$ must be taken high and low again for further serial data transfer. $\overline{SYNC}$ may be taken high after the falling edge of the 18th SCLK pulse, observing the minimum SCLK falling edge to $\overline{SYNC}$ rising edge time, t_6. If $\overline{SYNC}$ is taken high before the 18th falling edge of SCLK, the data transfer will be aborted and the addressed DAC will not be updated. See the timing diagram in Figure 1.

Daisy-Chain Mode (DCEN = 1)

In Daisy-Chain Mode, the internal gating on SCLK is disabled. The SCLK is continuously applied to the input shift register when $\overline{SYNC}$ is low. If more than 18 clock pulses are applied, the data ripples out of the shift register and appears on the D_{OUT} line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the D_{IN} input on the next device in the chain, a multidevice interface is constructed. Eighteen clock pulses are required for each device in the system. Therefore, the total number of clock cycles must equal 18N, where N is the total number of devices in the chain. See the timing diagram in Figure 2.

When the serial transfer to all devices is complete, $\overline{SYNC}$ should be taken high. This prevents any further data being clocked into the input shift register. A burst clock containing the exact number of clock cycles may be used and $\overline{SYNC}$ taken high some time later. After the rising edge of $\overline{SYNC}$, data is automatically transferred from each device's input shift register to the addressed DAC.

$\overline{RESET}$ Function

The $\overline{RESET}$ function on the AD5516 can be used to reset all nodes on this device to their power-on reset condition. This is implemented by applying a low going pulse of 20 ns minimum to the $\overline{RESET}$ Pin on the device.

Table III. Typical Power-On Values

Device	Output Voltage
AD5516-1	–0.073 V
AD5516-2	–0.183 V
AD5516-3	–0.391 V

$\overline{BUSY}$ Output

During conversion, the $\overline{BUSY}$ output is low and all SCLK pulses are ignored. At the end of a conversion, $\overline{BUSY}$ goes high indicating that the update of the addressed DAC is complete. It is recommended that SCLK is not pulsed while $\overline{BUSY}$ is low.

MICROPROCESSOR INTERFACING

The AD5516 is controlled via a versatile 3-wire serial interface that is compatible with a number of microprocessors and DSPs.

AD5516 to ADSP-2106x SHARC DSP Interface

The ADSP-2106x SHARC DSPs are easily interfaced to the AD5516 without the need for extra logic.

The AD5516 expects a t_3 ($\overline{SYNC}$ falling edge to SCLK falling edge setup time) of 15 ns min. Consult the *ADSP-2106x User Manual* for information on clock and frame sync frequencies for the SPORT Register and contents of the TDIV and RDIV Registers.

A data transfer is initiated by writing a word to the TX Register after the SPORT has been enabled. In write sequences, data is clocked out on each rising edge of the DSP's serial clock and clocked into the AD5516 on the falling edge of its SCLK. The SPORT transmit control register should be set up as follows:

DTYPE = 00, Right Justify Data
ICLK = 1, Internal Serial Clock
TFSR = 1, Frame Every Word
INTF = 1, Internal Frame Sync
LTFS = 1, Active Low Frame Sync Signal
LAFS = 0, Early Frame Sync
SENDN = 0, Data Transmitted MSB First
SLEN = 10011, 18-Bit Data-Words (SLEN = Serial Word)

Figure 6 shows the connection diagram.

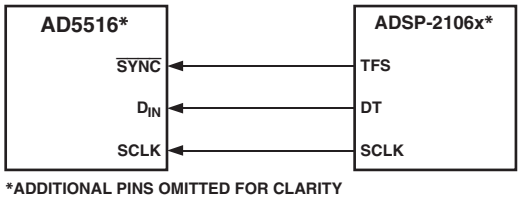

Figure 6. AD5516 to ADSP-2106x Interface

AD5516 to MC68HC11

The serial peripheral interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 0, and the Clock Phase Bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see the *68HC11 User Manual*. SCK of the 68HC11 drives the SCLK of the AD5516, the MOSI output drives the serial data line (D_{IN}) of the AD5516. The $\overline{SYNC}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5516, the $\overline{SYNC}$ line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to transmit 18 data bits, it is important to left justify the data in the SPDR Register. PC7 must be pulled low to start a transfer and taken high and low again before any further read/write cycles can take place. A connection diagram is shown in Figure 7.

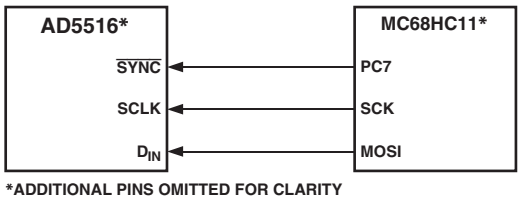

Figure 7. AD5516 to MC68HC11 Interface

AD5516 to PIC16C6x/7x

The PIC16C6x/7x synchronous serial port (SSP) is configured as an SPI master with the Clock Polarity Bit (CKP) = 0. This is done by writing to the Synchronous Serial Port Control Register (SSPCON). See the *PIC16/17 Microcontroller User Manual*. In this example, I/O port RA1 is being used to provide a $\overline{SYNC}$ signal and enable the serial port of the AD5516. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, three consecutive write operations are required. Figure 8 shows the connection diagram.

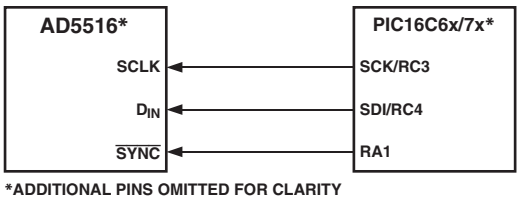

Figure 8. AD5516 to PIC16C6x/7x Interface

AD5516 to 8051

A serial interface between the AD5516 and the 80C51/80L51 microcontroller is shown in Figure 9. The AD5516 requires a clock synchronized to the serial data. The 8051 serial interface must therefore be operated in Mode 0. TxD of the microcontroller drives the SCLK of the AD5516, while RxD drives the serial data line. P1.1 is a bit programmable pin on the serial port that is used to drive $\overline{SYNC}$. The 80C51/80L51 provides the LSB first, while the AD5516 expects MSB of the 18-bit word first. Care should be taken to ensure the transmit routine takes this into account.

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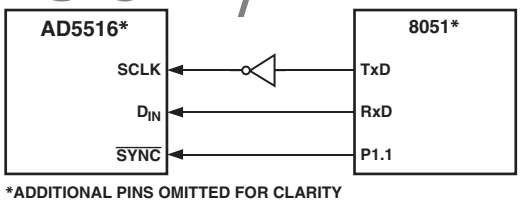

Figure 9. AD5516 to 8051 Interface

When data is to be transmitted to the DAC, P1.1 is taken low. Data on RxD is valid on the falling edge of TxD, so the clock must be inverted as the AD5516 clocks data into the input shift register on the rising edge of the serial clock. The 80C51/80L51 transmits its data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. As the DAC requires an 18-bit word, P1.1 must be left low after the first eight bits are transferred and brought high after the complete 18 bits have been transferred. DOUT may be tied to RxD for data verification purposes when the device is in Daisy-Chain Mode.

APPLICATION CIRCUITS

The AD5516 is suited for use in many applications, such as level setting, optical, industrial systems, and automatic test applications. In level setting and servo applications where a fine-tune adjust is required, the Mode 2 function increases resolution. The following figures show the AD5516 used in some potential applications.

AD5516 in a Typical ATE System

The AD5516 is ideally suited for the level setting function in automatic test equipment. A number of DACs are required to control pin drivers, comparators, active loads, parametric measurement units, and signal timing. Figure 10 shows the AD5516 in such a system.

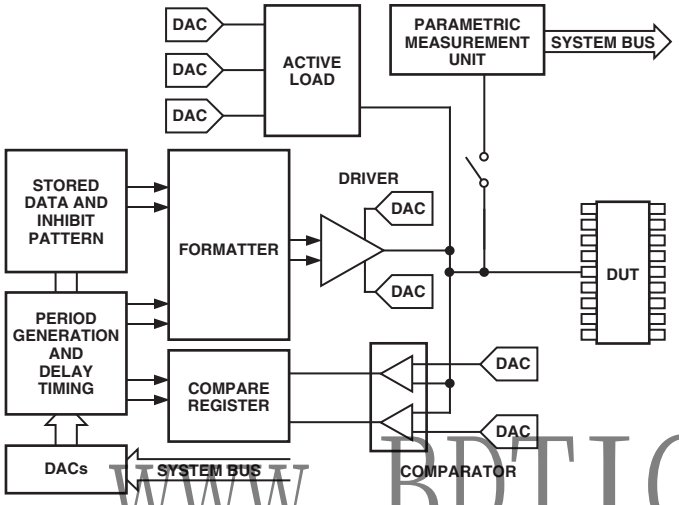

Figure 10. AD5516 in an ATE System

AD5516 in an Optical Network Control Loop

The AD5516 can be used in optical network control applications that require a large number of DACs to perform a control and measurement function. In the example shown in Figure 11, the outputs of the AD5516 are fed into amplifiers and used to control actuators that determine the position of MEMS mirrors in an optical switch. The exact position of each mirror is measured and the readings are multiplexed into an 8-channel, 14-bit ADC (AD7865). The increment and decrement modes of the DACs are useful in this application as they allow 14-bit resolution.

The control loop is driven by an ADSP-2106x, a 32-bit SHARC® DSP.

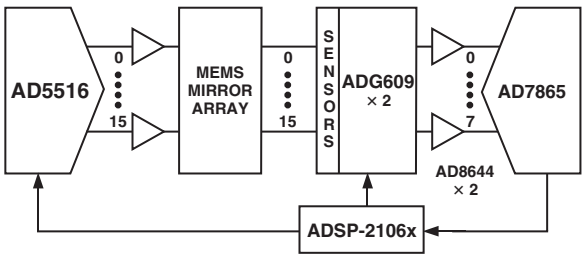

Figure 11. AD5516 in an Optical Control Loop

AD5516 in a High Current Circuit

Access to the feedback loop of the AD5516 amplifier provides greater flexibility, e.g., it enables the user to configure the device as a digitally programmable current source or increase the output drive current. See Figure 12. Note that V_{DD} must be chosen so that the DAC output has enough headroom to drive the BJT ~ 0.7 V above the maximum output voltage.

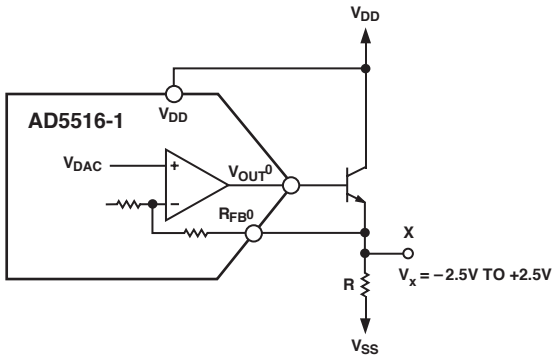

Figure 12. AD5516 in a High Current Circuit

Note it is not intended that the R_{FB} nodes be used to alter amplifier gain or for force/sense in remote sense applications.

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5516 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5516 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins ($AV_{CC}1$, $AV_{CC}2$), it is recommended to tie those pins together. The AD5516 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as closely to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

The power supply lines of the AD5516 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the D_{IN} and SCLK lines will help reduce crosstalk between them (not required on a multilayer board as there will be a separate ground plane, but separating the lines will help). It is essential to minimize noise on REFIN.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

As is the case for all thin packages, care must be taken to avoid flexing the package and to avoid a point load on the surface of the package during the assembly process.

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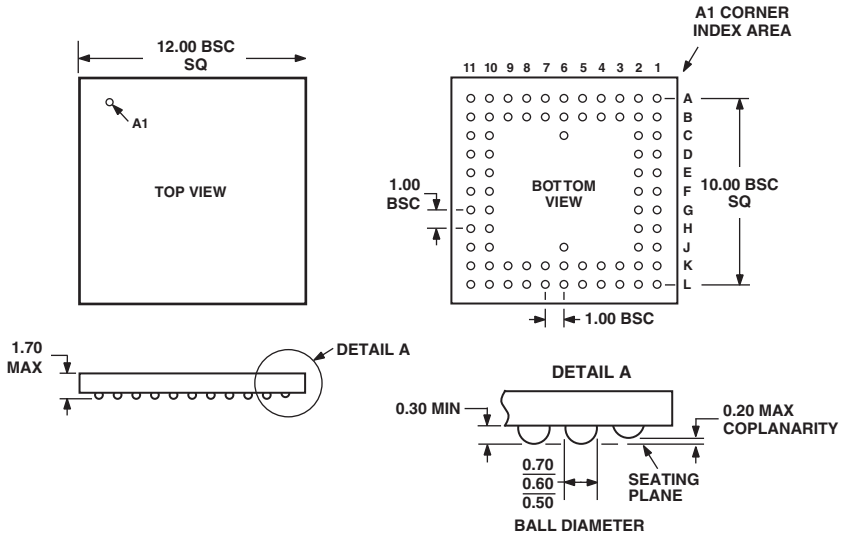
OUTLINE DIMENSIONS

74-Lead Chip Scale Ball Grid Array [CSPBGA]
(BC-74)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-192ABD-1

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Revision History

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Updated ORDERING GUIDE	5
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Addition of TPC 15	9
Changes to Mode 2 section	10
Changes to Figure 5	10
Changes to Figure 9	12
8/02—Data Sheet changed from REV. 0 to REV. A.	
Term LFBGA updated to CSPBGA	Global
Changes to SPECIFICATIONS	2
Addition to ORDERING GUIDE	5
Changes to FUNCTIONAL DESCRIPTION	10
Changes to DIGITAL-TO-ANALOG section	10
Added AD5516 in a High Current Circuit section	13
Added Figure 12	13
Updated BC-74 package	14

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